WHAT IS CLAIMED IS:

1. A multiple port crossbar for a communication switch, comprising:

first, second, and third crossbars, each of said crossbars including M ports; and

a plurality of interconnect buses, a first set of K ports of said first crossbar coupled to a first set of K ports of said second crossbar through K of said interconnect buses, a second set of K ports of said first crossbar coupled to a first set of K ports of said third crossbar through K of said interconnect buses, and a second set of K ports of said second crossbar coupled to a second set of K ports of said third crossbar through K of said interconnect buses, wherein L ports of each of said first, second and third crossbars are available as ports for said multiple port crossbar, and wherein $M > L > K$.

2. The multiple port crossbar of Claim 1, wherein $M = 12$, $L = 6$ and $K = 3$.

3. The multiple port crossbar of Claim 1, wherein each of said interconnect buses comprises a full duplex bus operating at approximately 2.88 Gigabits/second.

4. The multiple port crossbar of Claim 1, wherein each of said first, second and third crossbars is a 12-port crossbar chip.

5. The multiple port crossbar of Claim 4, wherein one of said interconnect buses is a chip-to-chip interconnect bus operating at approximately 2.88 Gigabits/second full duplex.

6. The multiple port crossbar of Claim 1, wherein each of said interconnect buses is a chip-to-chip interconnect bus.

7. The multiple port crossbar of Claim 1, provided as an ethernet crossbar.

8. An ethernet switch assembly comprising:

a multiple port crossbar including first, second, and third crossbars, each of said crossbars including M ports, and a plurality of interconnect buses, a first set of K ports of said first crossbar coupled to a first set of K ports of said second crossbar through K of said interconnect buses, a second set of K ports of said first crossbar coupled to a first set of K ports of said third crossbar through K of said interconnect buses, and a second set of K ports of said second crossbar coupled to a second set of K ports of said third crossbar through K of said interconnect buses, wherein L ports of each of said first, second and third crossbars are available as ports for said multiple port crossbar, and wherein $M > L > K$; and

a plurality of ethernet controllers each having a first input coupled to a respective one of said available ports of said multiple port crossbar via an interconnect bus.

9. The ethernet switch assembly of Claim 8, wherein $M = 12$, $L = 6$ and $K = 3$.

10. The ethernet switch assembly of Claim 8, wherein each of said plurality of ethernet controllers further have an output coupled to a PHY communication layer.

11. The ethernet switch assembly of Claim 8, wherein one of said interconnect buses comprises a full duplex bus operating at approximately 2.88 Gigabits/second.

12. The ethernet switch assembly of Claim 8, wherein each of said first, second and third crossbars is a 12-port crossbar chip.

13. The ethernet switch assembly of Claim 8, wherein one of said interconnect buses is a chip-to-chip bus operating at 2.88 Gigabits/second full duplex.

14. The ethernet switch assembly of Claim 8, wherein each of said interconnect buses is a chip-to-chip interconnect bus.

15. The ethernet switch assembly of Claim 8, wherein each of said interconnect buses coupling said crossbars is a chip-to-chip interconnect bus.

16. A method for increasing port availability for communication coupling from M port crossbars, comprising:

passing communication signals between a first set of K ports of a first M port crossbar and a first set of K ports of a second M port crossbar;

passing communication signals between a second set of K ports of said first M port crossbar and a first set of K ports of a third M port crossbar;

passing communication signals between a second set of K ports of said second M port crossbar and a second set of K ports of said third M port crossbar; and

sending any of said communication signals through any of L further ports of each of said first, second and third M port crossbars, wherein M > L > K.

17. The method of Claim 16, wherein M = 12, L = 6 and K = 3.

18. The method of Claim 16, wherein one of said passing steps includes passing said communication signals at approximately 2.88 gigabits/second full duplex.

20. The method of Claim 16, wherein all of said passing steps include passing said communication signals at approximately 2.88 gigabits/second full duplex.